METHOD AND APPARATUS FOR A REFERENCE CLOCK BUFFER SYSTEM

ABSTRACT

According to one example embodiment, a buffer, *e.g.*, in a clock/signal distribution apparatus is provided that substantially reduces jitter due to power supply noise. Decoupler and input stage isolates load from the top rail power supply (V_{DD}). In a more particular embodiment, jitter contributions from the bottom rail power supply (V_{SS}) can be minimized by cross-coupled load devices within load. Substantial independence from process and temperature is facilitated through the use of current bias, such as Proportional to Absolute Temperature (PTAT) current bias.